ABSTRACT

A DLL circuit having a phase comparison circuit for comparing phases of a reference clock and a delay clock and a variable delay addition circuit for adjusting delay amount according to a signal from the phase comparison circuit comprises a means for inputting a first signal latched at a logic "1" by start of 1 clock cycle of an internal clock to the variable delay addition circuit through a dummy delay at the start of burst and a means for detecting duration time of the logic "1" of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit based on the duration time.